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The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN CHIANG, SHASHANK MERCHANT,
and MICHAEL VENGCHONG LAU

Appeal No. 2003-1240
Application No. 09/304,964

ON BRIEF

Before KRASS, FLEMING, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 2-11 and 13-18, which are all the claims remaining in the application.

We reverse, and enter a new ground of rejection as authorized by 37 CFR § 41.50(b).

BACKGROUND

The invention is directed to a mechanism for allocating time slots for processing queues from various ports of a communication switch. Claim 2 is reproduced below.

> 2. A multiport data communication system for switching data packets between ports, the data communication system comprising:
>
> a plurality of receive ports for receiving data packets,
>
> a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,
>
> the decision making engine including:
>
> a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,
>
> logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and
>
> a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,
>
> wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

The examiner relies on the following reference:

Wu et al. (Wu)	5,771,234	Jun. 23, 1998 (filed Dec. 6, 1995)

Claims 2-11 and 13-18 stand rejected under 35 U.S.C. § 102 as being anticipated by Wu.

We refer to the Final Rejection (Paper No. 7) and the Examiner's Answer (Paper No. 15) for a statement of the examiner's position and to the Brief (Paper No. 14) and the Reply Brief (Paper No. 16) for appellants' position with respect to the claims which stand rejected.

OPINION

Section 102 rejection

Appellants argue, with respect to instant claim 2, that the rejection neglects to point out where Wu discloses a "scheduler." (Brief at 11-12.) Although the rejection purports that all the claims are "clearly anticipated" by Wu, the rejection does not, as appellants note, point out a clear disclosure of the scheduler requirements. The examiner does, however, provide reasoning in the "Response to Arguments" section of the Answer in support of why the artisan would have recognized that the apparatus disclosed by Wu inherently contains a scheduler that meets the requirements of instant claim 2.

"[I]f there is no request from the memory which stores data cells, as argued by the Appellant[s], the processor 200 in Fig. 8 would have no idea how to allocate time slots to data memory that have data cells; thus some of the time slots might be allocated to a memory that don't have data cells to [be] processed; in other words, there will be some empty cell timeslots in the transmission cycle." (Answer at 7.) The examiner does not identify the "memory" to which the arguments refer. In view of the

statement of the rejection and the remainder of the responsive arguments, the "memory" appears to be exemplified by FIFO 110, shown in Figure 7 of Wu.

Wu's FIFO's 110, 120, and 140 are contained within cell input unit (CIU) 100. Col. 13, l. 47 et seq. Processor 200 (Fig. 8) comprises a number of such CIU's. Col. 15, l. 55 et seq.

Instant claim 2 recites that the scheduler is configured to receive a request for a time slot from a queuing device (e.g., a FIFO) when the queuing device holds data to be processed by the logic circuitry. Processor 200 of Wu contains priority circuit 260, which sequences the outputting of cells from each of the output FIFO's 230, 240, and 250. Col. 16, ll. 26-65. Instant claim 2 also requires, however, that the plurality of queuing devices correspond to the plurality of receive ports, which might suggest (multiple instances of) FIFO 110, which receive (or receives) the cells from a cell source (e.g., col. 13, ll. 58-62).

However, Wu describes, in express terms, the scheduling of cells. Column 16, lines 26 through 65 describe how cells in output FIFO's 230, 240, and 250 are sequenced for output. Column 13, line 47 through column 15, line 54 describes how token generator circuits 160 and 170 transmit tokens to switches 130 and 150, and further describes the use of clock signals, to assign priority states to the cells produced by the particular source. The rejection does not explain how Wu's detailed disclosure of cell scheduling might meet the terms of instant claim 2, but relies on inherency -- i.e., what "must" be true of Wu's system.

We find that none of the FIFO's described by Wu necessarily corresponds to any particular receive port. Wu refers to a "cell source" as any hardware that produces cells for writing into an outgoing bitstream. Col. 3, ll. 22-40. Wu is directed to determining priority according to the type of source (col. 5, ll. 18-22; col. 3, l. 62 - col. 4, l. 33), such as "best effort" sources and variable bit rate sources (having mean and peak rates). The source, rather than traffic on a particular physical port, determines how the cells are prioritized and scheduled for transmission. The source may connect through virtual paths and virtual channels (col. 1, l. 61 - col. 2, l. 41), which need not map one-to-one with corresponding physical ports.

Since independent claim 8 contains similar limitations to those of claim 2 that have not been shown as expressly or inherently described by Wu, we do not sustain the rejection of claims 2 through 11. Further, we reverse, pro forma, the rejection of claims 13 through 18, since we are unable to ascertain the scope of base claim 13 for any meaningful comparison with the prior art. The reversal of claims 13 through 18 is for the reason that rejections of claims over prior art should not be based on speculation and assumptions as to the scope of the claims. See In re Steele, 305 F.2d 859, 862, 134 USPQ 292, 295 (CCPA 1962).

New ground of rejection

We enter the following new ground of rejection against the claims in accordance with 37 CFR § 41.50(b): Claims 13-18 are rejected under 35 U.S.C. § 112, second

paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

The recitation of "the receive port" in lines 2 through 3 of independent claim 13 lacks proper antecedent in the claim. Moreover, claim 13 is, at the least, misdescriptive of the disclosed invention. The claim recites that "a data queue representing each of the receive ports is assigned with at least one of the time slots." Appellants state (spec. at 13) that a single rules queue 102 may be assigned to each receive port of the IMS (integrated multiport switch) 12, but the same paragraph also refers to "multiple rules queue 102." The paragraph explains that rules queues 1 to 12 are provided for 10/100 MAC ports 1 to 12, a rules queue 13 may support gigabit MAC port 24, and a rules queue 14 may be assigned to expansion port 30. As described at pages 14 through 16 of the specification, IRC scheduler 104 (Fig. 4) arbitrates between the rules queues 102 to allocate time slots in each scheduling cycle. There is no clear disclosure of "a" single data queue that represents "each" (i.e., all) of the receive ports. Nor is it understandable how such a data queue might be assigned with "at least one" of the time slots consistent with the remainder of the method set forth in claim 13. The scope of the claim is thus indeterminate.

CONCLUSION

The rejection of claims 2-11 and 13-18 under 35 U.S.C. § 102 as being anticipated by Wu is reversed. A new rejection of claims 13-18 under 35 U.S.C. § 112, second paragraph is set forth herein.

This decision contains a new ground of rejection pursuant to 37 CFR § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)). 37 CFR § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 CFR § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED -- 37 CFR § 41.50(b)

ERROL A. KRASS
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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) APPEALS
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